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TECHNICAL REPORT

colour inside

Semiconductor devices –
Scan based ageing level estimation for semiconductor devices

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SEMICONDUCTOR DEVICES –

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IEC TR 63133, which is a technical report, has been prepared by IEC technical committee 47: Semiconductor devices.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
47/2405/DTR	47/2425/RVDTR

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

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INTRODUCTION

A semiconductor device has an important role in reliability-critical applications, e.g., space, air and road vehicles, medical equipment. Although new technology has improved performance, power efficiency, cost efficiency etc., but the reliability becomes a serious threat [1][1]. As can be seen in Figure 1, failure rate is decreases in early life, and low constant failure rate is preserved for a while, then wear out failure rate is increases significantly. Especially for reliability-critical applications, it is important to precisely monitor the ageing level to forewarn of any impending catastrophic failure. The semiconductor ageing is caused by negative/positive bias temperature instability, hot carrier injection, and time dependent dielectric breakdown, electro migration, and stress migration, etc. Path delay is known to be increased due to various ageing failures. Although a few ageing monitoring techniques have been developed [2 to 5], the ageing level has not been precisely diagnosed. For reliability-critical applications, the ageing level information can be utilized for taking adequate measures timely, e.g., device replacement, performance switching using dynamic voltage-frequency scaling. This document describes an efficient technique to monitor the ageing and characterize the ageing level.

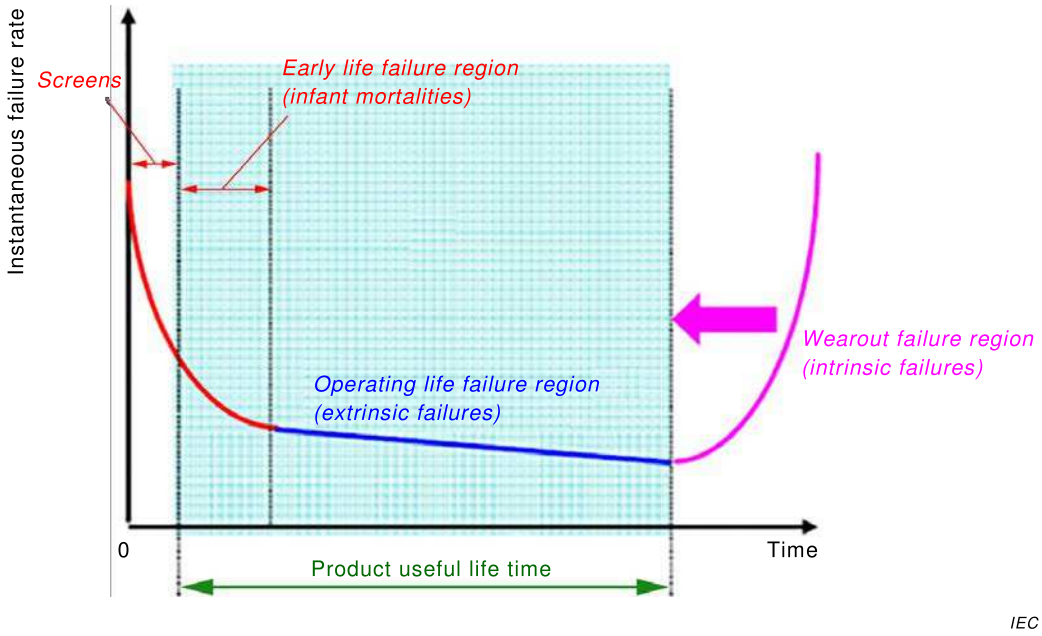

Figure 1 – Reliability bathtub curve

1 Numbers in square brackets refer to the Bibliography.

SEMICONDUCTOR DEVICES –

Scan based ageing level estimation for semiconductor devices

1 Scope

This Technical Report specifies a design technique of performance estimation storage element, which can monitor semiconductor ageing and characterize ageing level. The estimated ageing level can be used to improve the reliability of system.

2 Normative references

There are no normative references in this document.

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
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3.1.1
transistor ageing
for a field effect transistor, increase with time of its threshold voltage

Note 1 to entry: This increase is caused by a combination of NBTI, PBTI, HCI, TDDB, EM, and SM.

Note 2 to entry: This effect decreases the drain current and transconductance and thereby increases the path delay.

3.1.2
ageing level
degree of transistor ageing under known operating conditions

3.1.3
ageing level monitoring
method of evaluating transistor ageing that indicates either pass or fail at a selected ageing level

Note 1 to entry: The amount of delay between two clock signals corresponds to the selected ageing level.

Note 2 to entry: A path delay longer than the clock delay plus guard band constitutes a failure.

3.1.4
guard band
timing margin that allows for the worst acceptable increase of path delay through a device

3.1.5
scan cell
special purpose storage element employing design-for-testability, that is used for ageing level monitoring

Note 1 to entry: A scan cell may also be used as a functional storage element when not in test mode.

3.1.6
scan chain
chain of scan cells where the output of one is the input to the next

Note 1 to entry: This type of series connection is usually called as a daisy-chain.

3.1.7
test access port
port through which test equipment may be connected

Note 1 to entry: IEEE standard 1149.1 [6] specifies four (optionally five) lines for a TAP, i.e., test data input, test data output, test mode select, test clock and an optional test reset.

3.2 Abbreviations

3.2.1

CLK

CLocK

3.2.2

DFT

Design For Testability

3.2.3

EM

Electro migration

3.2.4

HCI

Hot carrier injection

3.2.5

NBTI

Negative bias temperature instability

3.2.6

PBTI

Positive bias temperature instability

3.2.7

PE

Performance evaluation

3.2.8
PECLK
Performance evaluation clock

3.2.9
PERC
Performance evaluation result cell

3.2.10
PESE
Performance evaluation storage element

3.2.11
PESI
Performance evaluation SI

3.2.12
PESO
Performance evaluation SO

3.2.13
SC
Scan cell

3.2.14
SE
Scan enable

3.2.15
SI
Scan input

3.2.16
SO
Scan output

3.2.17
SM
Stress migration

3.2.18
TAP
Test access port

3.2.19

TDDB

Time dependent dielectric breakdown

4 Ageing level

4.1 Overview

Semiconductor ageing is a serious threat to the reliability of a system. The ageing level of semiconductor components can be described as the degree of semiconductor ageing under certain operating conditions, including voltage, frequency, temperature, and usage rate. Over a certain lifetime of a semiconductor device, ageing is caused by several phenomena, including NBTI, PBTI, HCI, etc., and results in signal delay [7 to 9]. Therefore, the semiconductor ageing defect decreases the performance of a device, and ultimately causes system failure. Ageing should be precisely monitored and alarmed during functional operation for reliability. Thus, this document introduces the method to estimate the degree of ageing of a semiconductor device, in other words, the ageing-level.

4.2 Ageing level characterization technique (test method)

The ageing is modelled as a signal delay, and the ageing level can be estimated by monitoring the amount of induced delay at multiple delay points. The schematic of ageing level estimation technique can be described as in Figure 2. Normal and phase shifted clocks are applied to the device under ageing monitoring. Then the ageing level can be estimated through the ageing level analyser if any critical ageing failure is notified from the device.

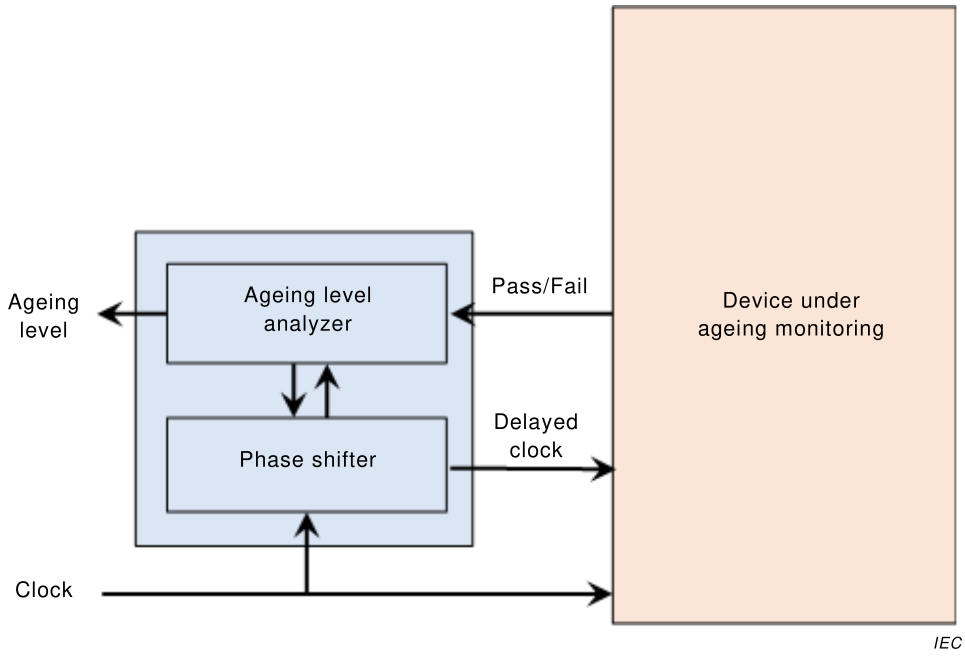


Figure 2 – Schematic of ageing level estimation technique

The monitoring range of the delay points for the ageing level is limited to the guard band as can be seen in Figure 3. The blue and red arrows indicate the ageing monitoring points representing the pass and fail in delay test, respectively. The amount of the ageing level can be estimated as the boundary value between blue and red arrows in which the delay test started to fail. As the device gets older, the ageing level becomes nearer to the rising edge of normal clock because more delay on the signal path due to the ageing causes earlier fail (red arrow) in the delay test.

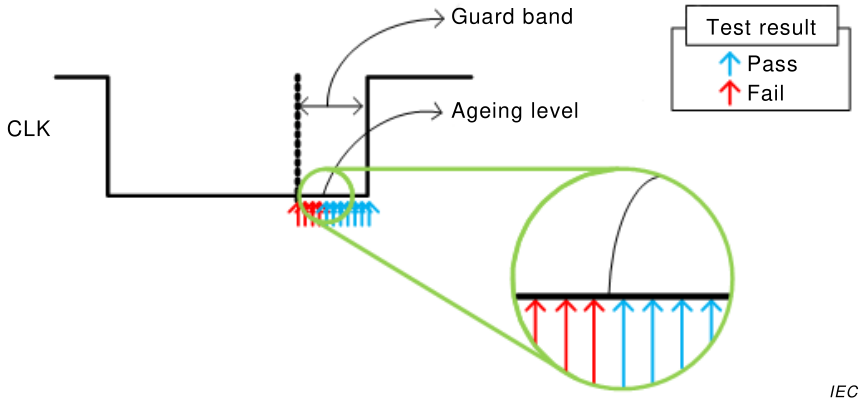
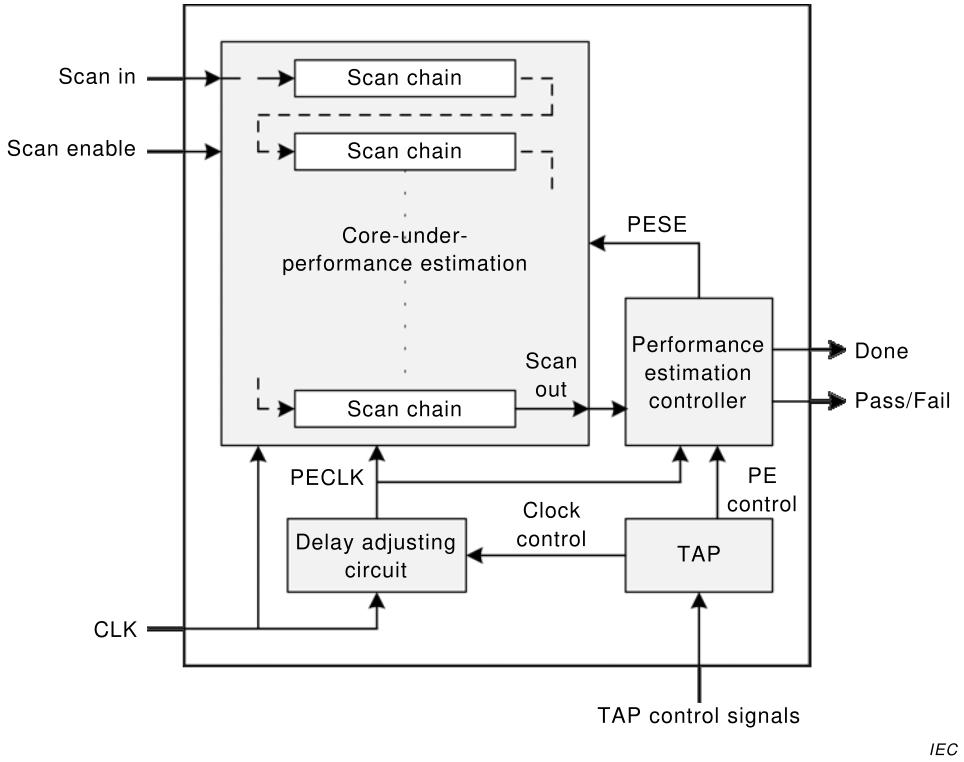


Figure 3 – A guard band and estimated ageing level

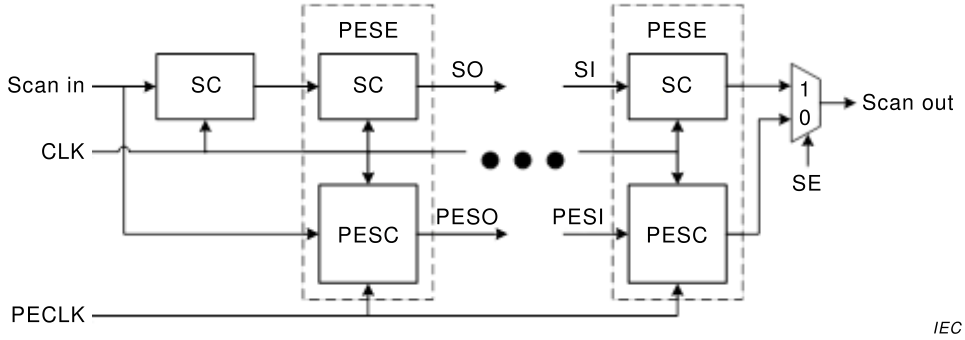
To implement this approach, a flexible ageing monitoring scheme is required that allows dynamic change of the ageing monitoring points; however, current techniques do not provide such a feature. This document proposes an efficient ageing monitoring scheme by using a shadow latch and phase-shifted clock. A shadow latch samples a signal earlier than the functional storage element through a phase-shifted clock in which the amount of phase shift is finely controlled. The sampled data with both the functional and phase-shifted clocks are compared to observe any path delay. The ageing level can be estimated by finely changing the amount of phase shift and monitoring any delay failure within the monitoring range.

In [2], the ageing is monitored with a single clock cycle of capture and multiple clock cycles of serial scan shift out. It is repeated multiple times because it is unlikely for a signal transition to be observed through a single capture cycle. However, in the proposed approach, after multiple capture cycles only a single shift out sequence is required. The results of multiple captures are compacted before unloading, hence the time to monitor the ageing multiple times can be significantly reduced.

4.3 Architecture and operation



(a) Ageing level monitoring architecture



(b) Scan chain architecture with scan cells and performance estimation scan cells

Figure 4 – Ageing level monitoring and scan chain architecture

Figure 4a) shows the architecture of the ageing level estimation process. The core-under-performance estimation has a scan chain, which is comprised of regular scan-cells and PESEs, as shown in Figure 4b). A PESE consists of an SC and PESC.

The PEC samples monitored results via a scan-out terminal and compares the results and after a complete monitoring process, it asserts the “Done” signal with a “Pass/Fail” signal. PEC settings include the scan chain length and the number of multiple captures; these are stored in decrement counters. PECLK is phase shifted version of CLK and generated via a delay-adjusting circuit. The amount of delay and PEC settings are shifted through an IEEE std. 1149.1 TAP controller.

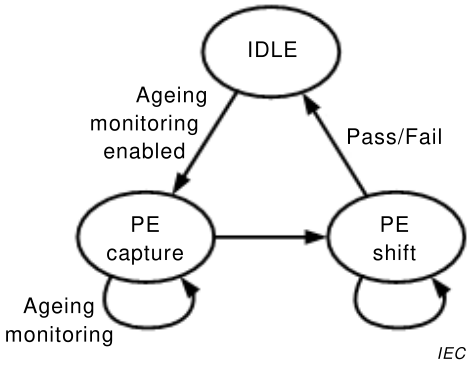
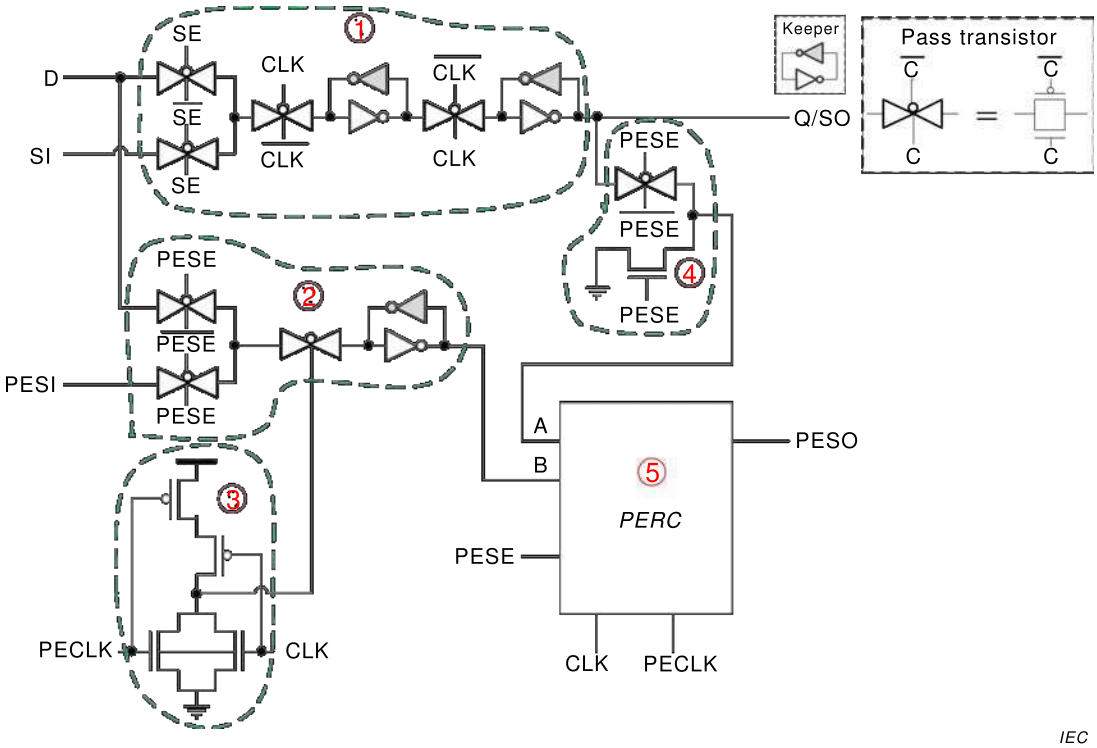


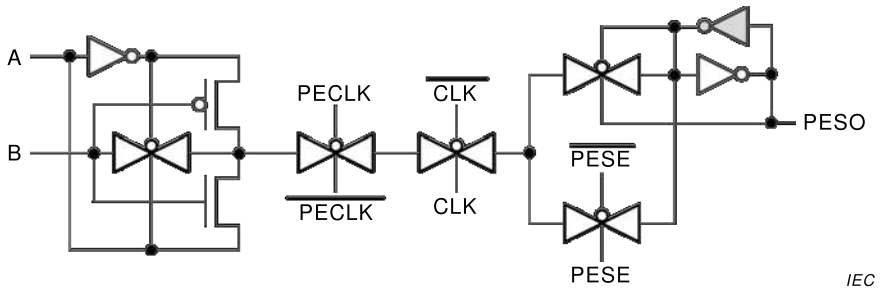
Figure 5 – State diagram for performance estimation controller

Figure 5 shows the state diagram for the PEC. By the ageing monitoring enable signal, the state changes from “IDLE” to “PE capture,” and PECLK is enabled. During this state, PESCs continuously sample until the counter for the monitoring capture becomes “0.” After finishing the captures, the state changes to “PE shift,” and the PESE signal changes to “1”. During this state, the results are unloaded through the scan chain to check the ageing status. After the counter for the shift operation becomes “0”, (1) the “Done” signal is set, (2) if ageing is detected, the Pass/Fail signal becomes “0” otherwise “1”, and (3) the next state becomes “IDLE”. To reduce power consumption during the “IDLE” state, all the monitoring cells can be turned off by keeping PECLK at “1” and loading “1” into each scan cell while unloading the capture results.

4.4 Performance estimation storage element



(a) Performance estimation storage element



(b) Performance estimation result cell

Figure 6 – Modified scan cell architecture

Figure 6 shows the proposed PESE architecture. The storage element, shadow latch, and PERC use keepers consisting of two inverters with different driving capabilities to retain the state [10]. A PESE consists of five parts: ① a scan storage element, ② a shadow latch, ③ a sampling time indicator, ④ a logic controlling the input A of PERC, and ⑤ a PERC that compares the values of A and B and then stores the result. The details of each part are described in the following:

① A scan storage element part is designed considering a scan design, and keepers are adopted in order to reduce the area overhead.

② A shadow latch part stores the value of either D or PESI chosen by PESE at specific timing which is elaborated in ③.

③ A sampling time indicator part receives CLK and PECLK, and then outputs “1” if both signals are “0,” which is equivalent as a NOR gate operation.

④ When PESE is “1,” it sets the input A value of PERC to be “0” indicating that PERC can work as a latch, otherwise the input A value of PERC becomes the value of output of storage element.

⑤ When the values of PESE, CLK and PECLK are “0,” “1” and “0,” respectively, the values of A and B are compared and stored into the keeper (this process is described as storing in PERC throughout this proposal). The compared result is stored only if the keeper’s previous value is “1.” When PESE “1,” the input A becomes “0” and the keeper stores the inverted value of B that is an inversion of PESI. In other words, the keeper of PERC, which is connected with PESO, stores the value of PESI.

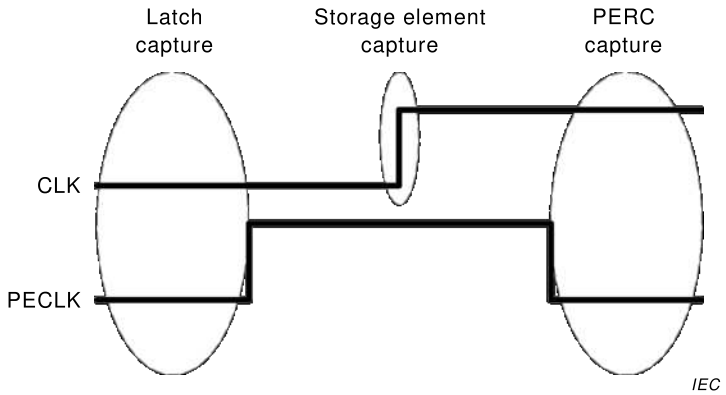


Figure 7 – Operations of shadow latch, storage element, and PERC according to CLK and PECLK

All of the PESE timings are adjusted by CLK and PECLK. Figure 7 shows a timing diagram for both clocks along with the corresponding operation. There are three storing points: (1) the data on D or PESI is latched into the shadow latch when both clocks are “0,” (2) the functional storage element samples at the rising edge of CLK, and (3) the stored data of the shadow latch and the functional storage element are compared, and the result is stored in PERC.

4.5 Simulation results

Here a simple simulation is conducted for easy understanding. A scan chain of eight cells was designed with the proposed PESEs and generated 8-bit parallel data for the scan chain to mimic an output of a combinational logic. It is assumed that the device is operated at 1 GHz during functional mode and the guard band is 10 %. Therefore, to estimate the ageing level in the simulation, the data were sampled 100 ps earlier than the rising edge of the functional clock.

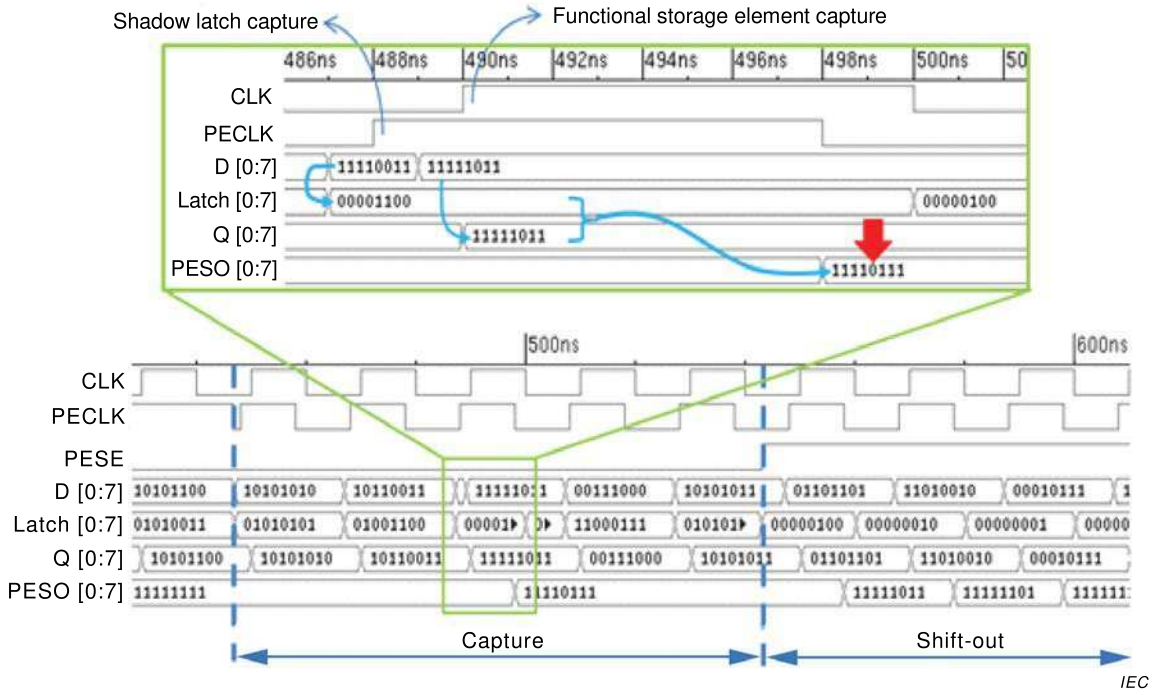


Figure 8 – Simulation results for a case in which ageing occurs on a data path

Figure 8 shows the simulation result. To verify the functionality of the proposed PESE, ageing was consciously induced in the fourth significant bit of the data through a delay. As represented by the red arrow, the fourth bit is transmitted (11110011 => 11111011) after capturing into the shadow latch. Thus, “11110011” is captured by PESEs when both clocks are zero, and “11111011” is captured by the functional storage elements (Q) at the rising edge of the CLK. When CLK and PECLK are “1,” “0,” respectively, the compared result is captured into the PERC that has same the value of PESO. Therefore, the first 8 bits in the PERC become “11110111,” which means ageing is detected on the fourth data path. Finally, the test results are shifted out and analysed.

4.6 Experimental results

Since a transistor ages gradually, a periodic ageing monitoring is more realistic and has the advantage of reducing power consumption [2]. The frequency of periodic monitoring should be increased as the device gets older. The monitoring frequency of a device through its life time can be effectively determined by considering the current ageing level but was fixed in previous approaches. The ageing level for each component is estimated based on the present performance, which varies according to the usage rate and environmental factors such as temperature, voltage, etc.

For periodic monitoring, a separate monitoring mode should be supported. Previous approaches either cannot support a separate monitoring mode [4, 5] or cannot effectively reduce the power consumption [2, 3]. However, the ageing estimating cell of the proposed storage element is appropriately controlled for reducing the power consumption.

The power consumptions are compared for three storage elements: the proposed storage element, the Ageing sensor storage element [2] and the Early capture storage element [3], during functional and ageing monitoring modes. These three storage elements are simulated through H-Spice using 50-nm technology BSIM library [11]. We applied random inputs to these storage elements for several milliseconds and measure the average power consumption. The results are presented in Table 1 and its first column specifies the type of storage element. The second column specifies the functional mode powers of each storage element and the last two columns list the capture and shift power during ageing monitoring mode. The results reveal that during functional mode, the proposed storage element significantly reduces the power consumption compared to other storage elements in which the early capture storage element remains on and the sensor of the ageing sensor storage element does not remain completely off during the functional mode. However, the proposed storage element slightly increases both the capture and shift power during ageing monitoring mode.

Table 1 – Power consumption compared with prior work

Storage element Type	**Functional Mode** (μW)	**Monitoring Mode** (μW)	
		Capture	**Shift**
Ageing sensor storage element [2]	7,22	9,84	-
Early capture storage element [3]	7,89	13,82	7,44
PESE (proposed)	3,90	13,04	8,05

Since the ageing monitoring mode is periodically activated for a very short time that is further shrunk with the proposed storage element due to multiple captures, the power increment during monitoring mode is negligible. Furthermore, it is noted that the average power consumption of the proposed storage element is significantly lower than other approaches.

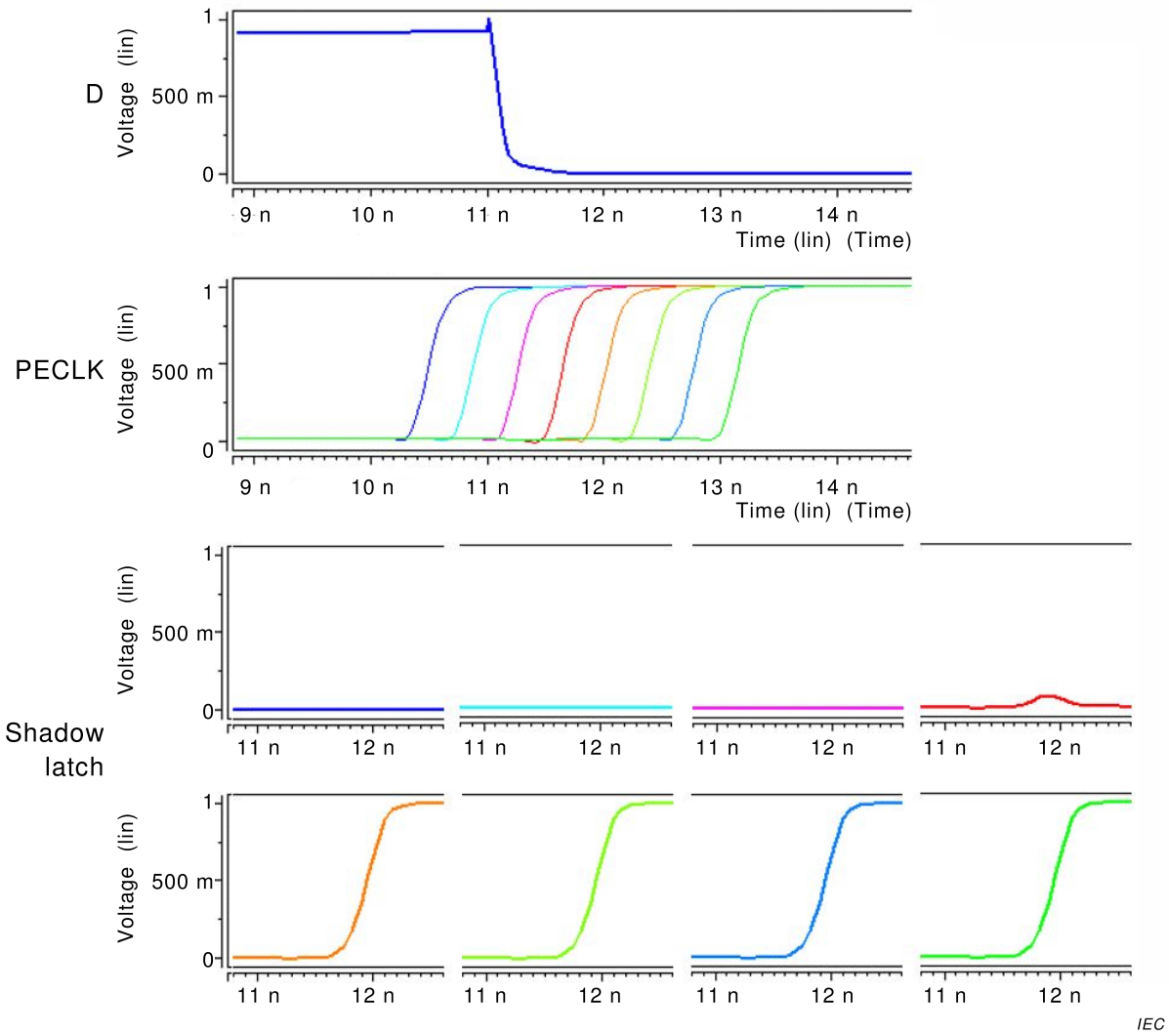


Figure 9 – PECLKs for various delay points and their results

Figure 9 shows PECLKs for various delay points and their results in shadow latches. A signal has arrived at 11 ns on the input D. The shadow latch is supposed to hold the inverted value of input D, hence the value of the shadow latch has to be high for ageing free PECLK in Figure 7. There are 8 phase shifted PECLKs and four of them (blue, sky, magenta, red) detect ageing. Therefore, the ageing level is estimated as the fifth PECLK (orange).

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